Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications

HiQ-CBR Series, C0G Dielectric, Low ESR
6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Overview

KEMET’s CBR Series surface mount multilayer ceramic capacitors (MLCCs) in C0G dielectric feature a robust and exceptionally stable copper electrode dielectric system that offers excellent low loss performance (high Q). These devices provide extremely low ESR and high self-resonance characteristics, and are well-suited for resonant circuit applications or those where Q and stability of capacitance characteristics are required. CBR Series capacitors exhibit no change in capacitance with respect to time and voltage, and boast a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to ±30 ppm/°C from −55°C to +125°C.

CBR Series devices are suitable for many circuit applications including RF power amplifiers, mixers, oscillators, low noise amplifiers, filter networks, antenna tuning, timing circuits, delay lines, and MRI imaging coils.

Benefits

- High Q and low ESR
- High SRF
- High thermal stability
- 1 MHz to 50 GHz frequency range
- Operating temperature range of −55°C to +125°C
- Base metal electrode (BME) dielectric system
- Pb-free and RoHS compliant
- 0201, 0402, 0603, and 0805 case sizes (inches)
- DC voltage ratings of 6.3 V, 10 V, 25 V, 50 V, 100 V, 200 V, 250 V, and 500 V
- Capacitance offerings ranging from 0.1 pF up to 100 pF

Ordering Information

<table>
<thead>
<tr>
<th>CBR</th>
<th>02</th>
<th>C</th>
<th>330</th>
<th>F</th>
<th>9</th>
<th>G</th>
<th>A</th>
<th>C</th>
<th>Packaging/Grade (C-Spec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series</td>
<td>Case Size (L&quot;x W&quot;)</td>
<td>Specification/Series</td>
<td>Capacitance Code (pF)</td>
<td>Capacitance Tolerance</td>
<td>Rated Voltage (VDC)</td>
<td>Dielectric</td>
<td>Termination Style</td>
<td>Termination Finish</td>
<td></td>
</tr>
<tr>
<td>CBR</td>
<td>02 = 0201, 04 = 0402, 06 = 0603, 08 = 0805</td>
<td>C = Standard</td>
<td>Two significant digits and number of zeros: Use 9 for 1.0 – 9.9 pF, Use 8 for 0.1 – 0.99 pF</td>
<td>A = ±0.05 pF, B = ±0.1 pF, C = ±0.25 pF, D = ±0.5 pF, F = ±1%, G = ±2%, J = ±5%</td>
<td>9 = 6.3 V, 8 = 10 V, 3 = 25 V, 5 = 50 V, 1 = 100 V, 2 = 200 V, A = 250 V, C = 500 V</td>
<td>G = C0G</td>
<td>A = N/A</td>
<td>C = 100% Matte Sn</td>
<td>Blank = 7&quot; Reel Unmarked</td>
</tr>
</tbody>
</table>

1 When ordering CBR Series devices, a “suffix” or “C-Spec” is not required to indicate a 7" reel packaging option. CBR devices are only available and shipped on 7" reels (paper tape). Bulk bag and cassette packaging options are not available. Please contact KEMET if you have a specific, non-standard packaging requirement.
Benefits cont.

- Available capacitance tolerances of ±0.05 pF, ±0.1 pF, ±0.25 pF, ±0.5 pF, ±1%, ±2%, and ±5%
- No piezoelectric noise
- No capacitance change with respect to applied rated DC voltage
- Negligible capacitance change with respect to temperature
- No capacitance decay with time
- Non-polar device, minimizing installation concerns
- 100% pure matte tin-plated termination finish allowing for excellent solderability

Applications

Typical applications include critical timing, tuning, bypass, coupling, feedback, filtering, impedance matching and DC blocking.

Field applications include wireless and cellular base stations, wireless LAN, subscriber-based wireless services, wireless broadcast equipment, satellite communications, RF power amplifier (PA) modules, filters, voltage-controlled oscillators (VCOs), PAs, matching networks, RF modules, satellite communications and medical electronics.

Qualification

RF and microwave products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4, Performance & Reliability.

Environmental Compliance

Pb-free and RoHS compliant.
Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications
HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Dimensions – Millimeters (Inches)

<table>
<thead>
<tr>
<th>Case Size (in.)</th>
<th>Case Size (mm)</th>
<th>L Length</th>
<th>W Width</th>
<th>T Thickness</th>
<th>B Bandwidth</th>
<th>Mounting Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>0201</td>
<td>0603</td>
<td>0.60±0.03 (0.024±0.001)</td>
<td>0.30±0.03 (0.012±0.001)</td>
<td>0.30±0.03 (0.012±0.001)</td>
<td>0.15±0.05 (0.006±0.002)</td>
<td>Solder Reflow Only</td>
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<tr>
<td>0402</td>
<td>1005</td>
<td>1.00±0.05 (0.040±0.002)</td>
<td>0.50±0.05 (0.020±0.002)</td>
<td>0.50±0.05 (0.020±0.002)</td>
<td>0.25±0.05/~0.10 (0.010±0.002/~0.004)</td>
<td>Solder Wave or Solder Reflow</td>
</tr>
<tr>
<td>0603</td>
<td>1608</td>
<td>1.60±0.10 (0.063±0.004)</td>
<td>0.80±0.10 (0.031±0.004)</td>
<td>0.80±0.07 (0.031±0.003)</td>
<td>0.40±0.15 (0.016±0.006)</td>
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<tr>
<td>0805</td>
<td>2012</td>
<td>2.00±0.20 (0.079±0.008)</td>
<td>1.25±0.20 (0.049±0.008)</td>
<td>0.85±0.10 (0.031±0.004)</td>
<td>0.50±0.20 (0.020±0.008)</td>
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Electrical Parameters/Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Parameters/Characteristics</th>
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</thead>
<tbody>
<tr>
<td>Operating Temperature Range:</td>
<td>−55°C to +125°C</td>
</tr>
<tr>
<td>Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC):</td>
<td>0 ±30 ppm/°C (0 ±60 ppm/°C for 0201 case size product ≥ 22 pF)</td>
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<tr>
<td>Aging Rate (Maximum % Capacitance Loss/Decade Hour):</td>
<td>0%</td>
</tr>
<tr>
<td>¹Dielectric Withstanding Voltage (DWV):</td>
<td>See Dielectric Withstanding Voltage Table (5±1 seconds and charge/discharge not exceeding 50 mA)</td>
</tr>
<tr>
<td>²Quality Factor (Q):</td>
<td>≥ 1,000 for capacitance values ≥ 30 pF</td>
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<tr>
<td></td>
<td>≥ 400 + 20°C for capacitance values &lt; 30 pF (C = Capacitance in pF)</td>
</tr>
<tr>
<td>³Insulation Resistance (IR) Limit at 25°C:</td>
<td>10 GΩ minimum (rated voltage applied for 120±5 seconds)</td>
</tr>
</tbody>
</table>

¹ DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

² Capacitance and quality factor (Q) measured at 1 MHz ±100 kHz and 1.0 ±0.2 Vrms.

³ To obtain IR limit, divide MD-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 & Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to “ON.”
Dielectric Withstanding Voltage Table

<table>
<thead>
<tr>
<th>Rated Voltage (VDC)</th>
<th>≤100 V</th>
<th>200 V</th>
<th>250 V</th>
<th>500 V</th>
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<tbody>
<tr>
<td>DWV</td>
<td>250%</td>
<td>200%</td>
<td>200%</td>
<td>150%</td>
</tr>
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</table>

Electrical Characteristics

SRF (MHz) vs. Cap (pF)
Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications

HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Electrical Characteristics cont.

ESR vs. Frequency 0402

<table>
<thead>
<tr>
<th>Freq (MHz)</th>
<th>1.8pF</th>
<th>4.7pF</th>
<th>10pF</th>
<th>18pF</th>
<th>22pF</th>
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<tbody>
<tr>
<td>2.2pF</td>
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<tr>
<td>10pF</td>
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<td>33pF</td>
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<td>47pF</td>
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<td>100pF</td>
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ESR vs. Frequency 0603

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<th>2.2pF</th>
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<th>10pF</th>
<th>20pF</th>
<th>47pF</th>
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<tbody>
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ESR vs. Frequency 0805

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<th>2.2pF</th>
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<th>33pF</th>
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<th>100pF</th>
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<td>4.7pF</td>
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<td>18pF</td>
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Q vs. Frequency 0402

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<th>10pF</th>
<th>18pF</th>
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Q vs. Frequency 0603

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<th>4.7pF</th>
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Q vs. Frequency 0805

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<th>Freq (MHz)</th>
<th>2.2pF</th>
<th>10pF</th>
<th>33pF</th>
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</tbody>
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# HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

## Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications

## Table 1 - CBR Series, Capacitance Range Waterfall

<table>
<thead>
<tr>
<th>Capacitance (pF)</th>
<th>Capacitance Tolerance</th>
<th>Capacitance Code (Available Capacitance)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
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<tr>
<td>0.2pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
</tr>
<tr>
<td>0.3pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
</tr>
<tr>
<td>0.4pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
</tr>
<tr>
<td>0.5pf</td>
<td>A = ±0.05 pF</td>
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<tr>
<td>0.6pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
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<tr>
<td>0.7pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
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<tr>
<td>0.8pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
</tr>
<tr>
<td>0.9pf</td>
<td>A = ±0.05 pF</td>
<td>B = ±0.1 pF</td>
</tr>
</tbody>
</table>

## Rated Voltage (VDC)

| 6.3 | 10 | 25 | 50 | 25 | 50 | 100 | 200 | 50 | 100 | 250 | 50 | 100 | 250 | 500 |
|-----|----|----|----|----|----|-----|-----|----|----|-----|----|----|-----|-----|-----|
| 6.3 | 10 | 25 | 50 | 25 | 50 | 100 | 200 | 50 | 100 | 250 | 50 | 100 | 250 | 500 |

*Available only in “B” (±0.1pF) capacitance tolerance.

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C1030_C0G_CBR • 7/9/2019

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<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Capacitance</th>
<th>Capacitance Code (Available Capacitance)</th>
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<tbody>
<tr>
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<tr>
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<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.25 pF</td>
<td>0.47 pF</td>
</tr>
<tr>
<td>0.47 pF</td>
<td>±0.5 pF</td>
<td>0.47 pF</td>
</tr>
</tbody>
</table>
Table 1 – CBR Series, Capacitance Range Waterfall cont.

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Capacitance Tolerance</th>
<th>Capacitance Code (Available Capacitance)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.6 pF</td>
<td>B  = ±0.1 pF</td>
<td>969</td>
</tr>
<tr>
<td></td>
<td>C  = ±0.25 pF</td>
<td>969</td>
</tr>
<tr>
<td></td>
<td>D  = ±0.5 pF</td>
<td>969</td>
</tr>
<tr>
<td>9.7 pF</td>
<td>G  = ±2%</td>
<td>979</td>
</tr>
<tr>
<td>9.8 pF</td>
<td>F  = ±1%</td>
<td>989</td>
</tr>
<tr>
<td>9.9 pF</td>
<td>J  = ±5%</td>
<td>999</td>
</tr>
<tr>
<td>10 pF</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>11 pF</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td>12 pF</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>13 pF</td>
<td></td>
<td>130</td>
</tr>
<tr>
<td>15 pF</td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>16 pF</td>
<td></td>
<td>160</td>
</tr>
<tr>
<td>18 pF</td>
<td></td>
<td>180</td>
</tr>
<tr>
<td>20 pF</td>
<td></td>
<td>200</td>
</tr>
<tr>
<td>22 pF</td>
<td></td>
<td>220</td>
</tr>
<tr>
<td>24 pF</td>
<td></td>
<td>240</td>
</tr>
<tr>
<td>27 pF</td>
<td></td>
<td>270</td>
</tr>
<tr>
<td>30 pF</td>
<td></td>
<td>300</td>
</tr>
<tr>
<td>33 pF</td>
<td></td>
<td>330</td>
</tr>
<tr>
<td>36 pF</td>
<td></td>
<td>360</td>
</tr>
<tr>
<td>39 pF</td>
<td></td>
<td>390</td>
</tr>
<tr>
<td>43 pF</td>
<td></td>
<td>430</td>
</tr>
<tr>
<td>47 pF</td>
<td></td>
<td>470</td>
</tr>
<tr>
<td>51 pF</td>
<td></td>
<td>510</td>
</tr>
<tr>
<td>56 pF</td>
<td></td>
<td>560</td>
</tr>
<tr>
<td>62 pF</td>
<td></td>
<td>620</td>
</tr>
<tr>
<td>68 pF</td>
<td></td>
<td>680</td>
</tr>
<tr>
<td>75 pF</td>
<td></td>
<td>750</td>
</tr>
<tr>
<td>82 pF</td>
<td></td>
<td>820</td>
</tr>
<tr>
<td>91 pF</td>
<td></td>
<td>910</td>
</tr>
<tr>
<td>100 pF</td>
<td></td>
<td>100</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Rated Voltage (VDC)</th>
<th>Voltage Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.3</td>
<td>9 8 3 5 3 5 1 2 5 1 A 5 1 A C</td>
</tr>
</tbody>
</table>
Table 2 – Chip Thickness/Reeling Quantities

<table>
<thead>
<tr>
<th>Chip Size</th>
<th>Chip Thickness (mm)</th>
<th>Reel Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>0201 (0603)</td>
<td>0.30 ±0.03</td>
<td>15,000</td>
</tr>
<tr>
<td>0402 (1005)</td>
<td>0.50 ±0.05</td>
<td>10,000</td>
</tr>
<tr>
<td>0603 (1608)</td>
<td>0.80 ±0.07</td>
<td>4,000</td>
</tr>
<tr>
<td>0805 (2012)</td>
<td>0.85 ±0.10</td>
<td>4,000</td>
</tr>
</tbody>
</table>

Contact KEMET for availability.

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC–7351 (mm)

<table>
<thead>
<tr>
<th>Case Size (Inches)</th>
<th>Case Size (mm)</th>
<th>Density Level A: Maximum (Most) Land Protrusion</th>
<th>Density Level B: Median (Nominal) Land Protrusion</th>
<th>Density Level C: Minimum (Least) Land Protrusion</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>C Y X V1 V2</td>
<td>C Y X V1 V2</td>
<td>C Y X V1 V2</td>
</tr>
<tr>
<td>0201</td>
<td>0603</td>
<td>0.38 0.56 0.52 1.80 1.00</td>
<td>0.33 0.46 0.42 1.50 0.80</td>
<td>0.28 0.36 0.32 1.20 0.60</td>
</tr>
<tr>
<td>0402</td>
<td>1005</td>
<td>0.50 0.72 0.72 2.20 1.20</td>
<td>0.45 0.62 0.62 1.90 1.00</td>
<td>0.40 0.52 0.52 1.60 0.80</td>
</tr>
<tr>
<td>0603</td>
<td>1608</td>
<td>0.90 1.15 1.10 4.00 2.10</td>
<td>0.80 0.95 1.00 3.10 1.50</td>
<td>0.60 0.75 0.90 2.40 1.20</td>
</tr>
<tr>
<td>0805</td>
<td>2012</td>
<td>1.00 1.35 1.55 4.40 2.60</td>
<td>0.90 1.15 1.45 3.50 2.00</td>
<td>0.75 0.95 1.35 2.80 1.70</td>
</tr>
</tbody>
</table>

**Density Level A:** For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of 0603(1608) and 0805 (2012) case sizes.

**Density Level B:** For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.

**Density Level C:** For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC–7351).

Image below based on Density Level B for an EIA 1608 case size.
Soldering Process

Recommended Soldering Technique:
- Solder wave or solder reflow for 0603 and 0805 case sizes
- 0201 and 0402 case sizes are limited to solder reflow only

Recommended Soldering Profile:
- KEMET recommends following the guidelines outlined in IPC/JEDEC J–STD–020

Recommended Solder Alloys:

<table>
<thead>
<tr>
<th>Alloy</th>
<th>Composition</th>
<th>Solidus</th>
<th>Liquidus</th>
</tr>
</thead>
<tbody>
<tr>
<td>In50</td>
<td>50 In, 50 Pb</td>
<td>180°C</td>
<td>209°C</td>
</tr>
<tr>
<td>In52</td>
<td>52 In, 48 Sn</td>
<td>118°C</td>
<td>118°C</td>
</tr>
<tr>
<td>Sn62</td>
<td>62.5 Sn, 36.1 Pb, 1.4 Ag</td>
<td>179°C</td>
<td>179°C</td>
</tr>
<tr>
<td>Sn63</td>
<td>63 Sn, 37 Pb</td>
<td>183°C</td>
<td>183°C</td>
</tr>
<tr>
<td>Pb-Free</td>
<td>95.5 Sn, 3.8 Ag, 0.7 Cu</td>
<td>217°C</td>
<td>217°C</td>
</tr>
<tr>
<td>Hi-Temp</td>
<td>5 Sn, 93.5 Pb, 1.5 Ag</td>
<td>296°C</td>
<td>301°C</td>
</tr>
<tr>
<td>Sn5</td>
<td>5 Sn, 95 Pb</td>
<td>308°C</td>
<td>312°C</td>
</tr>
</tbody>
</table>
### Table 4 – Performance & Reliability: Test Methods & Conditions

<table>
<thead>
<tr>
<th>Stress</th>
<th>Test or Inspection Method</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Terminal Strength</td>
<td>Pressurizing force: 0201 case size: 2N, 0402 &amp; 0603 case sizes: 5N, 0805 case size: 10N, Test time: 10±1 second</td>
<td>No visible damage or separation of termination system.</td>
</tr>
<tr>
<td>Vibration Resistance</td>
<td>Vibration frequency: 10 ~ 55 Hz/minimum, Total amplitude: 1.5 mm, Test time: 6 hours (Two hours each in three mutually perpendicular directions.)</td>
<td>No visible damage. Cap change and Q/DF: To meet initial specification</td>
</tr>
<tr>
<td>Solderability</td>
<td>Solder temperature: 235±5°C, Dipping time: 2±0.5 seconds</td>
<td>95% minimum coverage of termination finish.</td>
</tr>
<tr>
<td>Board Flex</td>
<td>Capacitor is mounted to a substrate which is flexed by means of ram at a rate of 1 mm per second until the deflection becomes 1 mm. (Deflection is maintained for 5±1 second) Store at room temperature for 24±2 hours before measuring electrical properties.</td>
<td>No visible damage. Capacitance change: within ±5.0% or ±0.5 pF, whichever is larger. (Capacitance change is monitored during flexure.)</td>
</tr>
<tr>
<td>Resistance to Soldering Heat</td>
<td>Solder temperature: 260±5°C, Dipping time: 10±1 second, Preheating: 120 to 150°C for 1 minute before immerse the capacitor in a eutectic solder, Store at room temperature for 24±2 hours before measuring electrical properties.</td>
<td>No visible damage. Capacitance change: within ±2.5% or ±0.25 pF, whichever is larger. Q/DF, IR and dielectric strength: To meet initial requirements. 25% maximum leaching on each edge.</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>5 cycles of steps 1 - 4:</td>
<td>No visible damage. Capacitance change: within ±2.5% or ±0.25 pF, whichever is larger. Q/DF, IR and dielectric strength: To meet initial requirements.</td>
</tr>
<tr>
<td>Step 1</td>
<td>Minimum operating temperature +0/~3</td>
<td>30 ±3</td>
</tr>
<tr>
<td>Step 2</td>
<td>Room temperature</td>
<td>2 ~ 3</td>
</tr>
<tr>
<td>Step 3</td>
<td>Maximum operating temperature +3/~0</td>
<td>30 ±3</td>
</tr>
<tr>
<td>Step 4</td>
<td>Room temperature (25°C)</td>
<td>2 ~ 3</td>
</tr>
<tr>
<td>Store at room temperature for 24±2 hours before measuring electrical properties.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Stress Test or Inspection Method Requirements

### Humidity (Damp Heat) Steady State

- Test temperature: 40±2°C
- Humidity: 90 ~ 95% RH
- Test time: 500 +24/−0 hours
- Store at room temperature for 24±2 hours before measuring electrical properties.

**Requirements**

- No visible damage.
- Capacitance change: within ±5.0% or ±0.5 pF, whichever is larger.
- Q/DF value:
  - Capacitance ≥ 30 pF, Q ≥ 350
  - Capacitance < 30 pF, Q ≥ 275+2.5°C
- IR: ≥ 1GΩ

### Humidity (Damp Heat) Load

- Test temperature: 40±2°C
- Humidity: 90 ~ 95% RH
- Test time: 500 +24/−0 hours
- Applied voltage: rated voltage
- Store at room temperature for 24±2 hours before measuring electrical properties.

**Requirements**

- No visible damage.
- Capacitance change: within ±7.5% or ±0.75 pF, whichever is larger.
- Q/DF value:
  - Capacitance ≥ 30 pF, Q ≥ 200
  - Capacitance < 30 pF, Q ≥ 100+10/3°C
- IR: ≥ 500MO

### High Temperature Life

- Test temperature: 125±3°C
- Applied voltage:
  - 200% of rated voltage (10 VDC ~ 250 VDC)
  - 150% of rated voltage (6.3 VDC and 500 VDC)
- Test time: 1,000 +24/−0 hours
- Store at room temperature for 24±2 hours before measuring electrical properties.

**Requirements**

- No visible damage.
- Capacitance change: within ±3.0% or ±0.3 pF, whichever is larger.
- Q/DF value:
  - Capacitance ≥ 30 pF, Q ≥ 350
  - Capacitance < 30 pF, Q ≥ 275+2.5°C
- IR: ≥ 1GΩ

### ESR

- The ESR should be measured at room temperature and tested at frequency 1±0.1 GHz.

#### 0201 Case Size

<table>
<thead>
<tr>
<th>Capacitance Range</th>
<th>ESR Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 pF ≤ Capacitance ≤ 1 pF:</td>
<td>&lt; 350 mΩ/pF</td>
</tr>
<tr>
<td>1.0 pF ≤ Capacitance ≤ 5.0 pF:</td>
<td>&lt; 300 mΩ</td>
</tr>
<tr>
<td>5.0 pF ≤ Capacitance ≤ 22.0 pF:</td>
<td>&lt; 250 mΩ</td>
</tr>
</tbody>
</table>

#### 0402 Case Size

<table>
<thead>
<tr>
<th>Capacitance Range</th>
<th>ESR Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 pF ≤ Capacitance ≤ 1 pF:</td>
<td>&lt; 350 mΩ/pF</td>
</tr>
<tr>
<td>1.0 pF ≤ Capacitance ≤ 5.0 pF:</td>
<td>&lt; 300 mΩ</td>
</tr>
<tr>
<td>5.0 pF ≤ Capacitance ≤ 100 pF:</td>
<td>&lt; 250 mΩ</td>
</tr>
</tbody>
</table>

#### 0603 Case Size

<table>
<thead>
<tr>
<th>Capacitance Range</th>
<th>ESR Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3 pF ≤ Capacitance ≤ 1 pF:</td>
<td>&lt; 1,500 mΩ</td>
</tr>
<tr>
<td>1.0 pF ≤ Capacitance ≤ 10 pF:</td>
<td>&lt; 250 mΩ</td>
</tr>
<tr>
<td>10 pF ≤ Capacitance ≤ 100 pF:</td>
<td>&lt; 200 mΩ</td>
</tr>
</tbody>
</table>

#### 0805 Case Size

<table>
<thead>
<tr>
<th>Capacitance Range</th>
<th>ESR Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3 pF ≤ Capacitance ≤ 1 pF:</td>
<td>&lt; 1,500 mΩ</td>
</tr>
<tr>
<td>1.0 pF ≤ Capacitance ≤ 10 pF:</td>
<td>&lt; 250 mΩ</td>
</tr>
<tr>
<td>10 pF ≤ Capacitance ≤ 100 pF:</td>
<td>&lt; 200 mΩ</td>
</tr>
</tbody>
</table>

The ESR should be measured at room temperature and tested at frequency 500±50 MHz.

**0201 case size, 22pF ≤ Cap ≤ 33pF: < 300 mΩ**
Storage and Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature—reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction

Detailed Cross Section

Termination Finish (100% Matte Sn)
Barrier Layer (Ni)
End Termination/External Electrode (Cu)
Inner Electrodes (Cu)
Dielectric Material (BaTiO₃ Based)
End Termination/External Electrode (Cu)
Barrier Layer (Ni)
Termination Finish (100% Matte Sn)

Marking

CBR series devices are supplied unmarked. If you require marked product, please contact KEMET for availability of a laser-marked option.
Tape & Reel Packaging Information

KEMET offers RF and Microwave Multilayer Ceramic Chip Capacitors packaged in 8 mm tape on 7” reels. This packaging system is compatible with all tape-fed automatic pick and place systems.

Table 5 – Carrier Tape Configuration (mm)

<table>
<thead>
<tr>
<th>EIA Case Size</th>
<th>Tape Size (W)*</th>
<th>Lead Space (P)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0201 – 0402</td>
<td>8</td>
<td>2</td>
</tr>
<tr>
<td>0603 – 1210</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>

*Refer to Figure 1 for W and P, carrier tape reference locations.  
*Refer to Table 6 for tolerance specifications.
Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications

HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Figure 1 – Punched (Paper) Carrier Tape Dimensions

Table 6 – Punched (Paper) Carrier Tape Dimensions
Metric will govern

<table>
<thead>
<tr>
<th>Tape Size</th>
<th>D₀</th>
<th>E₁</th>
<th>P₀</th>
<th>P₂</th>
<th>R Reference Note 2</th>
<th>K₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>1.55±0.05 (0.061±0.002)</td>
<td>1.55±0.05 (0.061±0.002)</td>
<td>4.0±0.10 (0.157±0.004)</td>
<td>2.0±0.05 (0.079±0.002)</td>
<td>25.0 (0.984)</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tape Size</th>
<th>Pitch</th>
<th>A₀</th>
<th>B₀</th>
<th>F</th>
<th>P₁</th>
<th>T</th>
<th>W</th>
<th>D₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>Half (2 mm)</td>
<td>0.37±0.03 (0.015±0.001)</td>
<td>0.67±0.03 (0.03±0.001)</td>
<td>0.62±0.05 (0.025±0.002)</td>
<td>1.12±0.05 (0.04±0.002)</td>
<td>3.5±0.05 (0.138±0.002)</td>
<td>2.0±0.05 (0.079±0.002)</td>
<td>0.42±0.03 (0.017±0.001)</td>
</tr>
<tr>
<td>8 mm</td>
<td>Single (4 mm)</td>
<td>1.00±0.10 (0.04±0.004)</td>
<td>1.80±0.10 (0.07±0.004)</td>
<td>4.0±0.10 (0.157±0.004)</td>
<td>0.95±0.05 (0.037±0.002)</td>
<td>8.0±0.10 (0.315±0.004)</td>
<td>0.95±0.05 (0.037±0.002)</td>
<td></td>
</tr>
</tbody>
</table>

2. The tape with or without components shall pass around R without damage (see Figure 3).
Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications
HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Packaging Information Performance Notes

1. **Cover Tape Break Force:** 1.0 Kg minimum.
2. **Cover Tape Peel Strength:** The total peel strength of the cover tape from the carrier tape shall be:

<table>
<thead>
<tr>
<th>Tape Width</th>
<th>Peel Strength</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>0.1 to 1.0 newton (10 to 100 gf)</td>
</tr>
<tr>
<td>12 and 16 mm</td>
<td>0.1 to 1.3 newton (10 to 130 gf)</td>
</tr>
</tbody>
</table>

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.

3. **Labeling:** Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. *Refer to EIA Standards 556 and 624.*

**Figure 2 – Bending Radius**

**Figure 3 – Tape Leader & Trailer Dimensions**
Surface Mount Multilayer Ceramic Capacitors (SMD MLCCs) for High Power Applications
HiQ-CBR Series, C0G Dielectric, Low ESR 6.3 – 500 VDC, 1 MHz – 50 GHz (RF & Microwave)

Figure 4 – Maximum Camber

![Carrier Tape](image1)
![Round Sprocket Holes](image2)

1 mm maximum, either direction

Figure 5 – Reel Dimensions

![Carrier Tape](image3)

Table 7 – Reel Dimensions
Metric will govern

<table>
<thead>
<tr>
<th>Tape Size</th>
<th>Reel Size</th>
<th>A</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>7</td>
<td>178±0.10</td>
<td>13.0±0.20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(7.008±0.004)</td>
<td>(0.512±0.008)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tape Size</th>
<th>N Minimum See Note 2, Table 6</th>
<th>W₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>60±0.10 (2.4±0.04)</td>
<td>8.4+1.5/−0.0 (0.331+0.059/−0.0)</td>
</tr>
</tbody>
</table>
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